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Voltage Controlled Delay Line with PFD for Delay Locked Loop in CMOS90nm Technology

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Abstract

Low power consumption is always desired for any electronic products today. Demand of modern measurement systems in submicron CMOS process introduced new challenges in design of low power high frequency clock generation systems. In the DLL Design, the performance of the VCDL is important part. Here the proposed architecture of VCDL can work at 1 GHz having different delay. In this paper, the proposedNOR based PFD have the better Jitter and Dead zone performance. The Jitter of the PFD is 76.4227 ps and Dead zone 32.3076 ps. The power consumption is 4.3530E-04 watts and having 20 transistors.

Keywords: Conventional Analog DLL, Proposed PFDarchitecture Proposed VCDL architecture

Introduction

In this high-speed generation and high-integration density systems, the synchronous adjustment between the different systems is very important. Asynchronous clock which were caused by the phase error would be a serious threat to the correctness of the operation of the whole circuit. The Phase Locked Loop (PLL) and Delay-Locked Loop (DLL) are the most commonly adopted to the purpose of clock synchronization. The locking time and the jitter performance are always the important consideration in the design of PLL and DLL [3]. Because DLL is a first order control system, it's more stable and easier to design. Moreover, PLL suffers from a later locking time and jitter accumulation due to the closed loop voltage-controlled oscillator (VCO). On the other hand, the DLL using the voltage-controlled delay line(VCDL) instead of the VCO does not accumulate over many clock cycles, therefore, DLL exhibits better jitter performance than PLL [3].

In addition, DLL have smaller area and faster locking time than the PLL.DLL can be classified into digital DLL, analog DLL, and mixed mode DLL [4], [5]. As far as the jitter performance is concerned, digital DLL is larger than the others since it suffers from quantization error. For mixed mode DLLincludes both analog DLL and digital DLL, its area of the chip is usually largest of all the others [3]. Compared with the digital DLL, the analog DLL has better jitter performance but it suffers from bigger chip area and later locking time

This paper is arranged as follows. Section II describes conventional Analog DLL. Section III gives the circuit description of Voltage Controlled Delay Line (VCDL). Section IV describes the circuit description of Phase Frequency Detector (PFD). Section V includes simulation results. Section VI concludes this paper.

Conventional Analog DLL

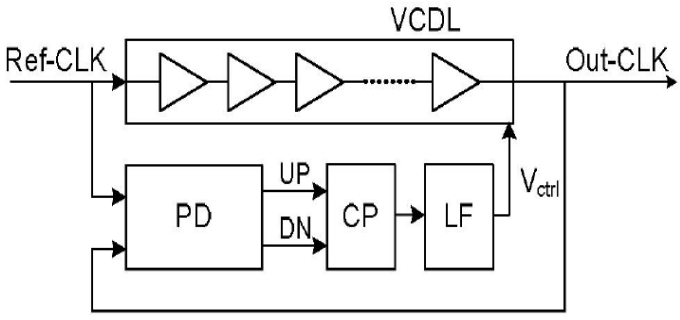

Figure (1) Conventional Analog DLL

A conventional DLL, as shown in Fig.1, consists of four major blocks: the Phase Detector (PD), the charge-pump circuit,the loop filter, and the VCDL. In the DLL, the referenceclock, ref_clk, is propagated through VCDL. The outputsignal,

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Vcdl_clk, at the end of the delay line is compared with the referenceinput. This is done by Phase detector and corresponding UP and DOWN signal generated. After that this signals goes to the inputs of charge pump. The charge pump generates the corresponding voltage and due to that the Low Pass Filter (LPF) is charged to some voltage. Depending to that voltage the delay of the VCDL is controlled. If delay different from integer multiples of clockperiod is detected, the closed loop will automatically correct itby changing the delay time of the VCDL [3].

The conventional DLL may suffer from harmonic locking or false locking over wide operating range.In order to overcome these problems, the delay time (T_{VCDL}) of the VCDL has a minimum and a maximum boundary between the periods (T_{CLK}) of the reference clock (ref_clk). Therefore, the minimum delay ($T_{VCDL.min}$) of the VCDL should be located between 0.5×TCLK and TCLK, and the maximum delay ($T_{VCDL.max}$), should be located between TCLK and 1.5×TCLK. On the other hand, the initial delay of VCDL needs to be located between 0.5×TCLK and 1.5×TCLK [18].

Voltage Controlled Delay Line

To overcome the problem of wide operating range, thefrequency ranges of the VCDL have to be large. Bychanging the number of delay cells in the delay line, the frequency range of the delay line can be increased. Architectures that are used in designing delay cells forvoltage-controlled delay line (VCDL) of a DLL can be categorized in two groups: full-swing that in many instances is named single-ended architecture andpartial-swing or differential pair configuration. Full swing delay cells can be current-starved. Important advantage of the partial-swing delay cells is higher frequency range. As previously mentioned switching number of delay cells in the VCDL to achieve a higher frequency range increases the total phase noise that is produced by the VCDL.

For given VCDL working frequency, the power dissipation, output voltage range and delay tuned range become the design limitations.The schematic of the current starved inverter used inthe voltage controlled Delay Line is shown in Figure 2. Inorder to minimize the sensitivity to supply and substrate noiseand to achieve a wide tuning range, the VCDL is built with aCurrent starved inverter (buffer) topology used in the AnalogDLL.

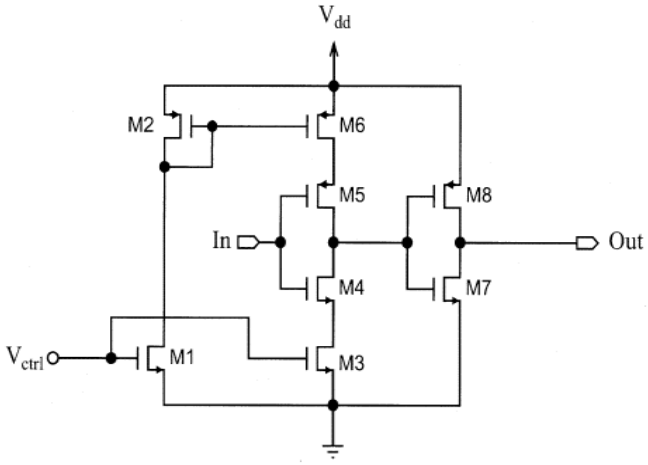

Figure (2) Current starved delay element

The control voltage Vctrl is applied to a series-connectedelement. The phase difference provided by each segment of VCDLdepends on the delay of each inverter.

It is most critical block of DLL, because VCDLs performance considerably affects the jitter of the output signal and the stability of the DLL. The Proposed architecture of VCDL is shown below figure (3).

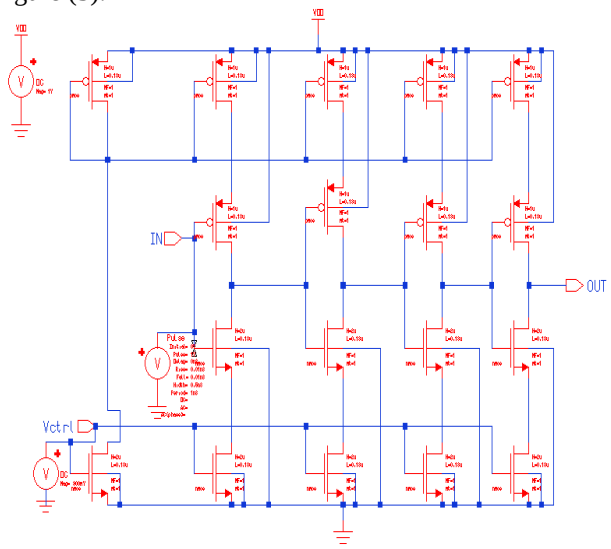

Figure (3) Proposed VCDL Architecture

Phase Frequency Detector

In addition to the voltage-controlled delay cells, the phase detector (PD) in the conventional DLL architecture is replaced by a phase/frequency detector (PFD) to achieve a sufficient locking range. The tuning precision of the DLL depends on the characteristics of the PFD. The widths of UP and DOWN pulses are proportional to the phase difference of the inputs as shown in Figure (4).

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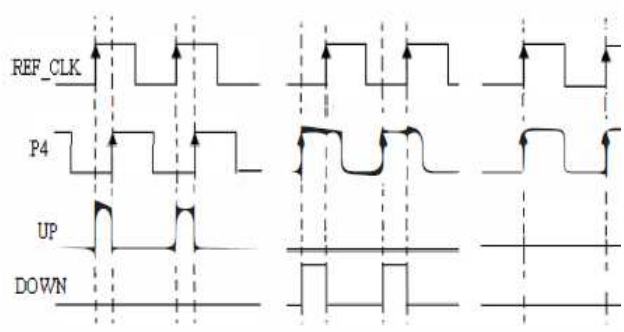

Figure (4) PFD operation

If the rising edge of the CLK leads the P4 rising edge, the UP output of the PFD goes high while the DOWN output remains low. If the P4 signal leads the CLK, UP remains low while the DOWN goes high and we can find the phase difference between P4 and CLK. In locked state, the both UP and DOWN output remains low.It compares the leading edges of REF_CLK and output of the Voltage Control Delay Line (VCDL) in DLL operation.

Figure (5) shows the PFD using NOR gate. The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a NOR Gate in the reset path. The REF and VCDL serve as clocks of the flip flops. The UPb and DNb signals are given as input to the NOR gate. Suppose the rising edge of REF leads that of VCDL, then UPb goes to logic low i.e. UP keeps high until the rising edge of VCDL makes DNb on low level. Because UPb and DNb are NORed, so RESET goes to logic high and resets the PFD into the initial state.

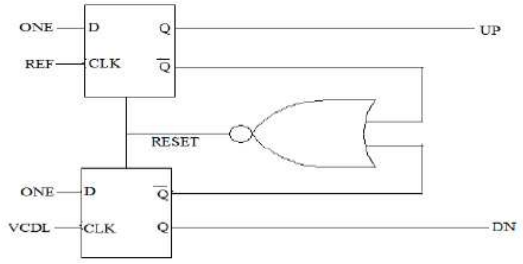

Figure (5) NOR Gate based PFD

The schematic of NOR gate PFD consisting of only 20 transistors is shown in figure (6).

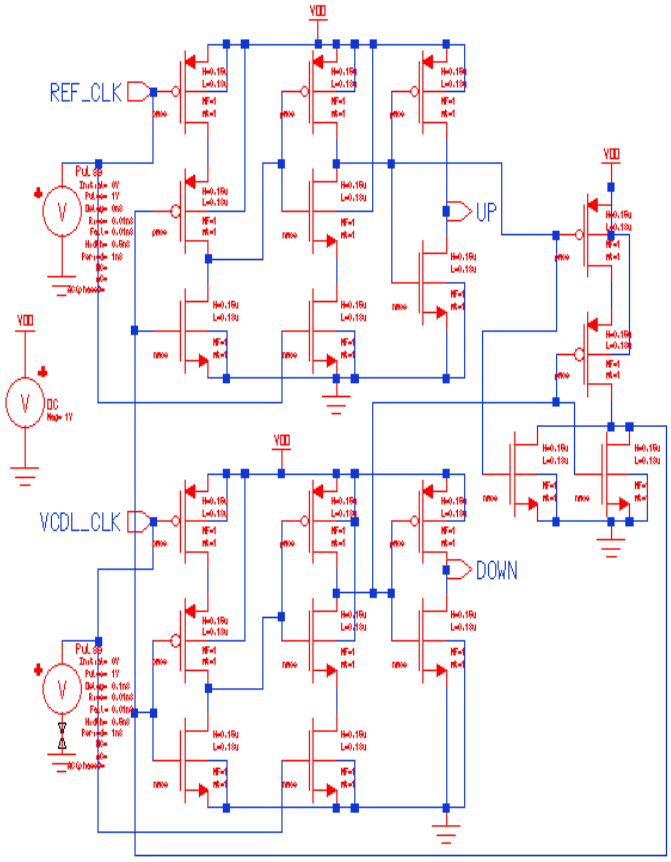

Figure (6) Schematic of NOR Gate based PFD

Simulation Results

The simulation result of Voltage Controlled Delay Line (VCDL) at 1GHz is shown in below figure (7).

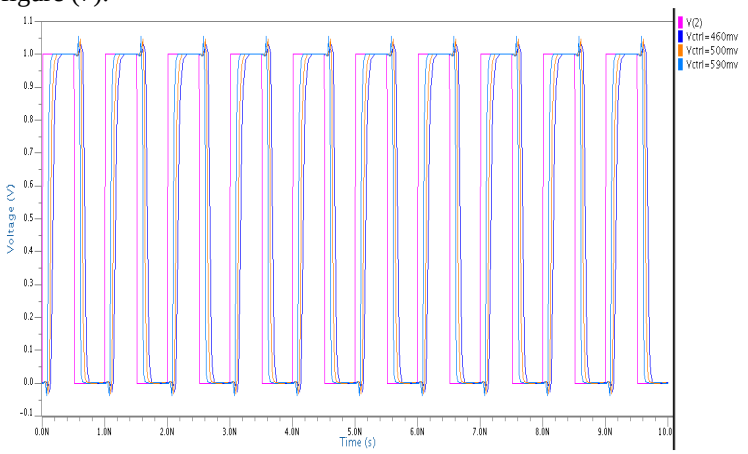

Figure (7) VCDL simulation at 1 GHz

The simulation result of the PFD at 1 GHz, where the rising edge REF_CLK leads the rising edge of the OUT_CLK, is shown in figure (8).

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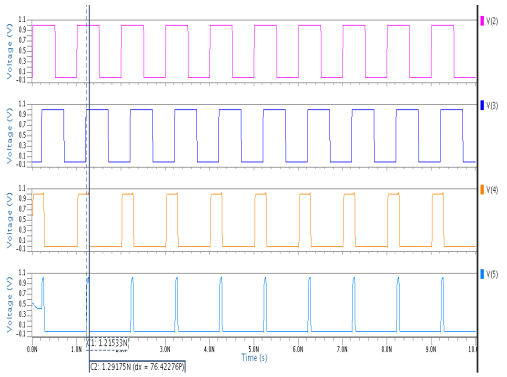


Figure (8) REF_CLK leads the OUT_CLK in PFD

The simulation result of the PFD in locking condition at 1 GHz is shown in figure (9).

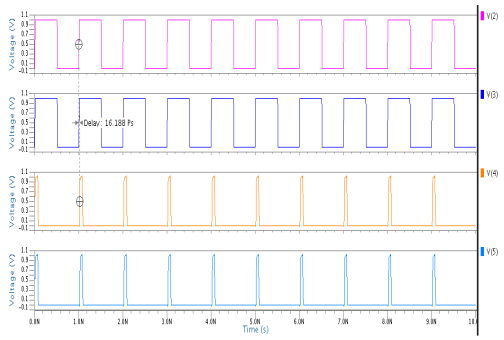


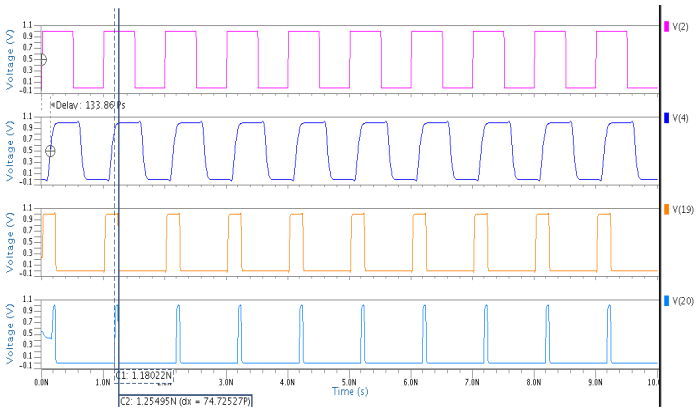
Figure (9) PFD in Lock state

Table 1 Shows the performance comparisons of the AND based PFD and NOR based PFD.

Table 1 Comparison of different PFDs

Parameters	AND based PFD	NOR based PFD
Max. Operation Frequency	1 GHz	1 GHz
Power Consumption	3.3022E-04 watts	4.3530E-04 watts
Transistor Counts	22	20
Dead zone	42.01 ps	32.3076 ps
Delay	21.871 ps	16.187 ps
Jitter	110.65 ps	76.4227 ps

The simulation result of the VCDL with PFD at 1 GHz, where the rising edge REF_CLK leads the rising edge of the VCDL output, is shown in figure (10).



Figure(10) VCDL with PFD (V_{ctrl} = 530mv)

Table 2. Shows the Delay and Jitter analysis of the VCDL & PFD, when I combine together.

V_{ctrl} (MHz)	Jitter	Delay
440	71.9697 ps	239.51 ps
460	69.9074 ps	204.36 ps
480	71.4285 ps	177.69 ps
500	73.1182 ps	155.61 ps
510	72.9508 ps	147.40 ps
520	72.6851 ps	140.30 ps
530	73.0769 ps	133.86 ps
560	72.8571 ps	117.39 ps
590	73.7704 ps	105.21ps

Conclusion

In order to extend the frequency range of analog DLLs a brand new delay cell is planned to use in coming up with the voltage-controlled delay line. The circuitsimulation is carried out by TSMC 0.18 um CMOS method. Simulation results show that the frequency rangeof the delay line that uses the new delay cell is increased up to 1GHz. The Jitter of the PFD is 76.4227 ps and Dead zone 32.3076 ps. The power consumption is 4.3530E-04 watts and having 20 transistors. The VCDL and PFD architecture matches with each other and generates required result as shown in figure (10).

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